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NBS TECHNICAL NOTE 773

Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report

October 1 to December 31, 1972

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Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report, October 1 to December 31, 1972

W. Murray Bullis, Editor

Electronic Technology Division
Institute for Applied Technology
National Bureau of Standards
Washington, D.C. 20234

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NBS Technical Notes are designed to supplement the Bureau's regular publications program. They provide a means for making available scientific data that are of transient or limited interest. Technical Notes may be listed or referred to in the open literature.

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FOREWORD

The Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices was undertaken in 1968 to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in methods of measurement for use in specifying materials and devices and in control of device fabrication processes. These improvements are intended to lead to a set of measurement methods which have been carefully evaluated for technical adequacy, which are acceptable to both users and suppliers, which can provide a common basis for the purchase specifications of government agencies, and which will lead to greater economy in government procurement. In addition, such methods will provide a basis for controlled improvements in essential device characteristics, such as uniformity of response to radiation effects.

The Program is supported by the National Bureau of Standards,* the Defense Nuclear Agency,† the U.S. Navy Strategic Systems Project Office,§ the Air Force Weapons Laboratory,+ the Air Force Cambridge Research Laboratories,¶ the Atomic Energy Commission,# and the National Aeronautics and Space Administration.** Although there is not a one-to-one correspondence between the tasks described in this report and the cost centers through which the Program is supported, the concern of certain sponsors with specific parts of the Program is reflected in planning and conduct of the work.

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* Through Research and Technical Services Cost Centers 4251126, 4252128, and 4254115.

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METHODS OF MEASUREMENT FOR SEMICONDUCTOR MATERIALS, PROCESS CONTROL, AND DEVICES

QUARTERLY REPORT
OCTOBER 1 TO DECEMBER 31, 1972

This quarterly progress report, eighteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include (1) completion of the investigation of the effects of current, probe force, and surface condition on the measurement of resistivity of bulk silicon wafers by the four-probe method, (2) establishment of operating conditions appropriate for determining the sensitivity of transient thermal response measurements to voids in transistor die attachment, and (3) initiation of an interlaboratory comparison of transistor scattering parameter measurements. Because of the general applicability of the first of these, details are presented in a separate appendix. Work is continuing on measurement of resistivity of semiconductor crystals; characterization of generation-recombination-trapping centers in silicon; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; measurement of thermal properties of semiconductor devices; determination of S-parameters, delay time, and related carrier transport properties in junction devices; development of a-c probing techniques; and characterization of noise and conversion loss of microwave detector diodes. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendices.

Key Words: Base transit time; carrier lifetime; delay time; die attachment; electrical properties; electronics; epitaxial silicon; four-probe method; generation centers; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; probing techniques (a-c); pull test, recombination centers; resistivity; resistivity standards; semiconductor devices; semiconductor materials; semiconductor process control; silicon; S-parameters; switching transients; thermal resistance; thermally stimulated measurements; trapping centers; wire bonds.

1. INTRODUCTION

This is the eighteenth quarterly report to the sponsors of the Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices. It summarizes work of a wide variety of measurement methods that are being studied at the National Bureau of Standards. The Program is a continuing one, and the results and conclusions reported here are subject to modification and refinement.

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Section 3 deals with tasks on methods of measurement for materials; section 4, with those on methods of measurement for process control; and section 5, with those on methods of measurement for devices. References for each section are listed in a separate subsection at the end of that section.

The report of each task includes the long-term objective, a narrative description of progress made during this reporting period, and a listing of plans for the immediate future. Additional information concerning the material reported may be obtained directly from individual staff members identified with the task in the report. The organization of the Joint Program staff and telephone numbers are listed in Appendix A.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix B suggests the extent of this participation. Additional details of current standardization activities not associated with a particular task are given in section 2.

Background material on the Program and individual tasks may be found in earlier reports in this series as listed in Appendix D. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix D. Reprints or copies of such publications are usually available on request to the author.

2. HIGHLIGHTS

Significant accomplishments during this reporting period include (1) completion of the investigation of the effects of current, probe force, and surface condition on the measurement of resistivity of bulk silicon wafers by the four-probe method, (2) establishment of operating conditions appropriate for determining the sensitivity of transient thermal response measurements to voids in transistor die attachment, and (3) initiation of an interlaboratory comparison of transistor scattering parameter measurements. Because of the general applicability of the first of these, details are presented in a separate appendix.

Highlights of these and other on-going activities are presented in this section; details of progress in technical areas are given in subsequent sections of the report. This section includes a summary of standardization activities being carried out by program staff members and concludes with a brief description of new technical efforts to be undertaken next quarter.

Resistivity — The results of the investigation of the four-probe method suggest that with well-maintained equipment 1) measurements can be made on specimens 10-Ω·cm and lower under a wide range of conditions including lapped, mechanically polished, and chem-mechanically polished surfaces and lower than standard probe force without significant loss of precision, 2) lapped surfaces are preferred for measurements on specimens with resistivity in the 100-Ω·cm range, and 3) most of the time (90 percent at a 90 percent confidence level) a single measurement will yield a value within ±1 percent of the average obtained by making 12 measurements under the same conditions.

Two silicon crystals have been ordered for use as standard reference wafers for four-probe resistivity measurements. One crystal has a nominal resistivity of 0.1 Ω·cm; the other, 10 Ω·cm. It is expected that the resistivity of each wafer can be provisionally certified, based on individual measurement, to ±5 percent. Initial sets of standards are scheduled to be available about July 1.

Generation-Recombination-Trapping Centers — Calculations made to determine detection conditions associated with measurements of thermally stimulated properties indicate that defects can be detected only in the upper half of the forbidden energy gap in p^+n junctions and only in the lower half of the forbidden energy gap in n^+p junctions. The results of heat treatment studies suggest that iron is being introduced into high resistivity silicon slices during or before gold diffusion.

Gold-Doped Silicon — The activation energy of the gold acceptor in silicon was obtained from measurements of the Hall coefficient as a function of temperature on a phosphorus-doped specimen with an initial resistivity of 75 Ω·cm. Spreading resistance measurements made on a boron-doped, gold-diffused silicon wafer to determine the uniformity of the gold diffusion as a function of depth showed a constant

resistance in the center region with the expected increase in resistance due to excess gold at depths up to 15 to 20 μm from the surface.

Infrared Methods — Infrared response measurements (IRR) on the 85 germanium specimens collected for the germanium study were completed. The tentative determination of the position within the forbidden energy gap of energy levels detected by IRR in germanium and silicon has been accomplished. The results are in very good agreement with summaries reported in the literature of energy levels detected by various methods after radiation or thermal damage.

Die Attachment Evaluation — Infrared microradiometer measurements on a number of previously investigated diodes with controlled voids indicated that the percent increase in peak junction-to-case temperature difference of diodes with voids over that of their respective controls, measured under steady-state conditions, correlated well with the electrical steady-state thermal response measurements. The infrared measurements also confirmed a previously noted trend that the sensitivity to void sizes of both 20 and 40 percent of the chip bonding area was nearly the same.

Measurements of thermal response made on transistor chips with 40 percent void area in the transistor die attachment indicated that there was no advantage, with respect to void sensitivity, of measuring the devices in the diode-connected transistor operating mode over that of the normal transistor operating mode. When the transistors were measured in the transistor operating mode, transient thermal response measurements made with a 5-ms wide heating power pulse were nearly seven times more sensitive to the presence of voids than were the steady-state thermal response measurements.

Wire Bond Evaluation — Further measurements of pull strength as a function of loop height for two-level bonds indicate that the variability in the experimental results observed to date may be due to substrate fabrication problems. Analysis of results on annealed single-level wire bonds indicates that elongation of the wire during pulling and subsequent increase in bond loop height probably accounts for the observed differences between experiment and theory.

Thermal Properties of Devices — Measurements of peak junction temperature were made with an infrared microradiometer on a group of transistors on which thermal resistance had been previously measured by both the emitter-only and the emitter-and-collector switching techniques. In both cases the measurements were made under conditions such that there were no severe current constrictions or hot spots. In most cases, the junction-to-case thermal resistance calculated from electrical measurements by the emitter-only switching technique extrapolated to 1 μs after the termination of the heating power pulse was within 10 percent of that determined from the infrared measurement. Further investigations were made into the mechanism of

the emitter-base voltage and current transients which occur when switching the emitter with a series transistor during measurement of thermal resistance by the emitter-only switching technique.

Microwave Device Measurements — Additional sensitivity relations were developed to estimate systematic measurement uncertainty. To assess repairs made to the modulation attenuator, it was operated repeatedly while observations were made of the variations in voltage output from a calorimeter used to monitor the power level. Analysis of the data indicated that the variability of attenuator setting was not responsible for most of the power variation.

Carrier Transport in Junction Devices — The S-parameters of three of the six special high-frequency probe assemblies for electrical probing of transistors at the wafer stage were measured over the frequency range 0.2 to 2 GHz. The upper limit of transistor delay-time error caused by inductance in the collector-base circuit of the vector voltmeter apparatus was computed. Five of the participants in the interlaboratory test of S-parameter measurements completed their transistor and passive network measurements; the sixth completed measurement of the passive networks and is beginning the transistor measurements.

Standardization Activities — Standardization activities directly related to particular task areas are reported with the appropriate tasks. However, many of the standardization activities undertaken by program staff are broader than the technical tasks described in the following sections. These activities, which are reported here, involve general staff support in committees, coordination of efforts which may encompass a variety of tasks, and participation in areas where no direct in-house technical effort is underway.

There was no scheduled meeting of ASTM Committee F-1 on Electronics this quarter. In addition to the activity reported in section 3.1., one document was edited, revisions were made in two documents in response to comments at the September meeting, and Hall effect measurements were made on eight gallium arsenide specimens as part of an interlaboratory test conducted by the Compound Semiconductors Section.

A program staff member attended meetings of SAE Committee H on Electronic Materials and Processes in Washington on October 31 and November 1. Discussions were directed toward development of a focus for the committee activity.

To provide liaison to the newly formed Subcommittee on Quality and Hardness Assurance in ASTM Committee F-1, a staff member attended meetings of ASTM Subcommittee F-10.07 on Radiation Effects on Electronic Materials in New Orleans on December 4 and 5.

New Directions — Considerable interest in improvements in measurement technology for control of device fabrication processes has been expressed recently by several organizations. Accordingly plans have been made to conduct, during the first six months of 1973, a field survey of the status of measurement technology now in use by the industry and of the needs in this area as identified by device manufacturers and users. In addition, new facilities are being set up to permit expanded in-house activity in this area. These include an automatic probe for spreading resistance measurements, an infrared camera system for viewing crystal defects, a scanning electron microscope for studying inspection and test techniques, and improved processing facilities.

3. SEMICONDUCTOR MATERIALS

3.1. RESISTIVITY

Objective: To develop methods suitable for use throughout the electronics industry for measuring resistivity of bulk, epitaxial, and diffused silicon wafers.

Progress: Two silicon crystals were ordered for use as standard reference wafers for four-probe resistivity measurements. Analysis of the results of the experimental study of the effects of current, probe force, and surface condition on the measurement of resistivity of bulk silicon wafers by the four-probe method was completed. Work continued on modification of specimen preparation, measurement conditions, and analysis for the capacitance-voltage method.

Silicon Resistivity Standards — Two *p*-type silicon crystals have been ordered to NBS specifications for use as resistivity standards. One crystal is to have a nominal resistivity of 0.1 Ω·cm; the other, 10 Ω·cm. It is expected that the resistivity of each wafer can be provisionally certified, based on individual measurement, to ±5 percent. Details of the multilaboratory collaborative experiment intended to establish the level to which such standards can ultimately be certified are being worked out. (J. R. Ehrstein and F. H. Brewer)

Other Standards Activities — Work continued on the round-robin experiment being conducted in conjunction with ASTM Committee F-1 on Electronics to determine the interlaboratory precision for four-probe resistivity measurements on silicon epitaxial layers deposited on substrates of opposite conductivity type. Subsequent to measurement by the eighth of the participating laboratories, the specimens were remeasured at NBS. Examination revealed that two *p/n* wafers which had yielded erratic results at the three previous laboratories were cracked. The ninth laboratory withdrew from the round robin so the experimental work is now complete. A final tabulation and analysis of the data is being made. (F. H. Brewer)

A recommended practice for a general procedure for measuring and adjusting the forces applied to the pins of a four-probe array during resistivity measurements was written for submission to the Resistivity Section of Committee F-1. The procedure is based on information developed during operation of the apparatus reported previously (NBS Tech. Note 743, pp. 8-9) and on procedures supplied by several other members of the Committee. (W. M. Bullis)

Four-Probe Method — Analysis of the results of the experimental study of the effects of current, probe force, and surface condition on the measurement of resistivity of bulk silicon wafers by the four-probe method was completed. In the study, measurements were made at five current levels (0.1, 0.22, 1.0, 2.2, and 10 times the

recommended value [1]) and four-probe forces (25, 40, 100, and 150 gf*) on six p-type wafers with resistivity in the range 0.001 to 100 Ω·cm spaced at about decade intervals and one 100-Ω·cm n-type wafer. The wafers were successively mechanically polished with 0.3-μm alumina, chem-mechanically polished [2], and lapped with 5 μm alumina. Except for a few isolated instances, variability in excess of ±2 percent, the stated three-sigma precision of the standard method [1], was not observed. The results are discussed in detail in Appendix E. (J. R. Ehrstein)

Capacitance-Voltage Methods — Changes were implemented in the junction fabrication process, in order to minimize the contact resistance and residual impurity contamination in the boron-diffused, n-type, homogeneous silicon p^+-n junctions used in the study of the capacitance-voltage (C-V) method. A phosphorus diffusion cycle, which creates an n^+ layer on the bottom of the wafer and a phospho-silicate glass on the top, is performed after the p^+ and oxide layers introduced during the boron diffusion have been removed from the bottom of the wafer by lapping. The glass layer on the top of the wafer acts as a getter for residual heavy metal contamination. The n^+ layer, in conjunction with a film of gold, which is next evaporated and alloyed to the bottom of the wafer, provides a low resistance contact to the n- region of the junction. The gold film can also serve as a diffusion source to fabricate gold-doped junction structures for future tests.

The test masks being used allow the fabrication of 20- and 60-mil (0.5- and 1.5-mm) diameter p-n junctions and MOS capacitors. These test structures have metal gates which allow the surface surrounding each test structure to be electrically controlled. Junctions have been fabricated in 0.2- and 30-Ω·cm n-type slices. Blank slices with the same resistivities were simultaneously diffused along with patterned slices for the purpose of measuring the diffused layer sheet resistance and junction depths. These parameters are needed for the C-V impurity profile program.

(M. G. Buehler and T. F. Leedy)

A new computer program was developed for use in profiling circular planar diffused junctions which have a complementary error function (erfc) diffusion profile. The surface concentration and junction depth are presumed to be known from the diffused layer sheet resistance and an angle lap and stain measurement. Corrections for both edge effects and depletion in the diffused layer are included in the manner described by Buehler [3] for Gaussian diffusion profiles. (R. L. Mattis)

A new electrical test station for C-V measurements was constructed. The test station features a gold-plated vacuum chuck mounted on an x-y stage insulated from ground. The stage accommodates a wafer up to 2 in. (51 mm) in diameter. A tungsten

*0.24, 0.39, 0.98, and 1.47 N, respectively.

wire spring is used to contact diffused layers, and a second probe is used to apply bias to the gates of gated diodes. A microscope is mounted above the x-y stage. The entire unit is housed in a metal box which shields against light and electrical signals. All electrical leads are coaxially shielded as close to the contacts as possible. (R. L. Mattis and A. W. Stallings)

Plans: The two crystals intended for resistivity standards will be screened for uniformity when received. If satisfactory, the necessary wafer fabrication and calibration measurements will commence. It is anticipated that the wafers will be available for sale by July 1, and that announcement of availability will be made both through electronics industry trade literature and through government publications. The analysis of the round-robin experiment on measurement of the resistivity of epitaxial layers by the four-probe method will be completed. Design of an experiment to test the effects of current, probe force, and probe tip condition on four-probe resistivity measurements on 5- and 25-μm thick *n*- and *p*-type epitaxial layers will be initiated. Silicon wafers fabricated by the new process will be profiled by the C-V method and the results compared to those obtained by the four-probe method. If the agreement is good, additional wafers at other resistivity levels will be prepared and measured. The new error function C-V impurity profile program will be compared to the Gaussian program to see if the results differ significantly.

3.2. GENERATION-RECOMBINATION-TRAPPING CENTERS

Objective: To develop electrical measurement methods including mathematical models and test structures for characterizing the electronic properties and density of generation-recombination-trapping (GRT) centers in silicon with emphasis on methods applicable to control of parameters such as lifetime and leakage current.

Progress: Calculations made to determine detection conditions associated with measurements of thermally stimulated properties indicate that defects can be detected only in the upper half of the forbidden energy gap in p^+n junctions and only in the lower half of the forbidden energy gap in n^+p junctions. Study of the open circuit voltage decay method continued. The results of heat treatment studies suggest that iron is being introduced into high resistivity silicon slices during or before gold diffusion.

Thermally Stimulated Properties — The basis for measurement of these properties is the ability to charge and discharge defect centers [1]. For a p^+n junction with acceptor defects on the *n*-side of the junction, the capacitance, C_2, during the discharge [2] following the charging of defects is given by

$$C_2 = \{(N_d - n_t)(q\varepsilon A^2)/[2\ (V_2 - V_1)]\}^{1/2} \qquad (1)$$

where V_1 is the bias at which the junction was charged, V_2 is the bias during the discharge, q is the electronic charge, ϵ is the dielectric constant, A is the junction area, N_d is the donor density on the *n*-type side of the junction, and n_t is the density of electrons on acceptor defects. The time dependent terms are C_2 and n_t. If the acceptor defects are assumed to be fully charged initially ($n_{ti} = N_t$) and fully discharged finally ($n_{tf} = 0$), the ratio of the defect density, N_t, to the donor density, N_d, is

$$\frac{N_t}{N_d} = \frac{C_{2f}^2 - C_{2i}^2}{C_{2f}^2} \tag{2}$$

where C_{2i} is the initial value of C_2 and C_{2f} is the final value. This is the optimum detection condition for the junction. If $n_{ti} \neq N_t$ or $n_{tf} \neq 0$, less than optimum detection conditions (ODC) prevail and $(N_t/N_d) > (C_{2f}^2 - C_{2i}^2)/C_{2f}^2$.

A measurement criterion, M, can be defined as

$$M = \frac{N_d}{N_t} \frac{C_{2f}^2 - C_{2i}^2}{C_{2f}^2} = \frac{n_{ti} - n_{tf}}{N_t [1 - (n_{tf}/N_d)]} \quad . \tag{3}$$

For optimum detection conditions, M = 1; when M = 0, no measurement is possible. The position of the Fermi energy, E_f, with respect to the defect energy, E_t, dictates the initial density of electrons on the defects

$$n_{ti} = N_t/\{1 + \exp[(E_t - E_f)/kT]\} \tag{4}$$

where k is Boltzmann's constant and T is the absolute temperature. The final density of electrons on the defects is governed by the hole and electron emission rates, e_p and e_n,

$$n_{tf} = e_p N_t/(e_n + e_p). \tag{5}$$

The quantity M is illustrated as a function of defect energy in figure 1 for an N_t/N_d ratio of 10^{-3} and various typical values of the emission coefficients, B_n and B_p, which are found in the expressions

$$e_n = B_n T^2 \exp[(E_t - E_c)/kT] \tag{6a}$$

and

$$e_p = B_p T^2 \exp[(E_v - E_t)/kT] \tag{6b}$$

where E_c and E_v are the energies of the conduction and valence band edges, respectively. Five regions are identified. In region I, the defect lies above the Fermi energy, M ≈ 0, and the defect cannot be observed. In the transition, region II, $E_f \approx E_t$, and n_{ti} is a rapidly varying function of trap energy. In region III, M = 1 and optimum detection conditions obtain. In region IV, $e_n \approx e_p$ so the defect does

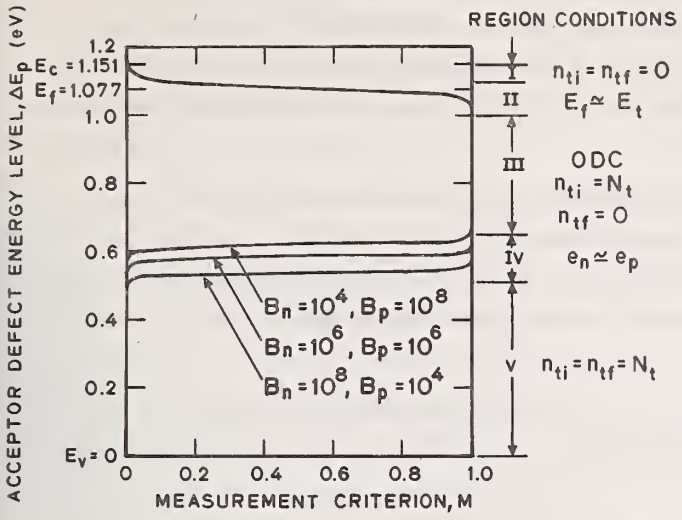

Figure 1. Criterion for detection by measurement of thermally stimulated properties of acceptor defects on the n-side of a p^+n junction at 100 K. (The defect density is 0.001 times the shallow donor density.)

not become fully discharged; this condition obtains within several kT of the midgap energy. In region V, $e_n << e_p$ so the defect remains charged at all times.

Since similar relationships apply for donor defects in p^+n junctions, one can conclude that defects must lie in the upper half of the forbidden energy gap for good detection conditions to exist. Analogous arguments apply to n^+p junctions where defects must lie in the lower half of the gap for good detection conditions to exist.

(M. G. Buehler and R. L. Mattis)

Open-Circuit Voltage Decay Method — If a forward biased p-n junction is suddenly open circuited, the initial part of the voltage decay transient is often observed to decay linearly with time. Lederhandler and Giacoletto [3] concluded that the slope of the linear part of the voltage decay transient (dV/dt) was related to an effective minority carrier lifetime, τ_e, by the relation

$$\tau_e = -\frac{kT}{q}\left(\frac{dV}{dt}\right)^{-1} \qquad (7)$$

where k is Boltzmann's constant, T is absolute temperature, and q is the electronic charge. Choo and Mazur [4] developed a general expression for the decay of mobile charge carriers in a p-n diode of arbitrary base width, W. From their analysis and experimental results it can be inferred that for base width shorter than several times the diffusion length, L, the geometry must be considered in calculating the lifetime for the decay transient. Preliminary calculations indicate that for small signal conditions and for $W/L \geq 5$, eq (7) may be used to predict lifetime provided that $V >> kT/q$. Expressions valid for $W/L < 5$ are under study.

The results of the OCVD experiments indicate that the slope of the linear portion of the OCVD transient is independent of current level. Also, it was noted that

when a diode was shunted with a resistor, the duration of the OCVD transient was shortened, but the slope of the linear part of the voltage decay was unaffected. Throughout all of the OCVD experiments a more or less linear voltage decay transient was always observed. (D. C. Lewis and M. G. Buehler)

Heat Treatment Studies — Additional electrical measurements were made on a specimen cut from a wafer previously heat treated at 1250°C for 8 h in an argon ambient as part of a study (NBS Tech. Note 743, p. 15) to determine the effects of temperature cycling during gold diffusion on the electrical properties of silicon (see Section 3.3.).

The specimen was boron-doped with an initial room temperature resistivity of 2300 Ω·cm, and was *n*-type with a resistivity of 3.8×10^4 Ω·cm following heat treatment. An activation energy of 0.53 eV was determined from a plot of the product of the Hall coefficient and the three-halves power of the temperature as a function of inverse temperature over the range 200 to 400 K. This energy is close to the value of 0.55 eV reported by Collins and Carlson [5] for the upper donor level of iron in silicon. Although this energy is also similar to that of the gold acceptor, presence of the latter would not result in the observed conversion from *p*- to *n*-type.

Minority carrier lifetime measurements were made by the surface photovoltage method on specimens cut from the wafers in the heat treatment study and compared with lifetime data obtained on untreated wafers cut from the same crystals. The reductions in lifetime following heat treatment ranged from factors of 5 to 500 depending on the specific treatment; at a given time and temperature, heat treatment in argon atmosphere resulted in a lower lifetime than the same treatment in an oxygen atmosphere. Such reductions are consistent with the presence of an efficient recombination center deep in the forbidden gap.

The results reported above suggest that extremely minute amounts of iron, introduced during the preparation of wafers for diffusion, are likely to be responsible for the observed resistivity and type changes in high resistivity *p*-type silicon. (W. R. Thurber and A. W. Stallings)

Surface Photovoltage Method — To obtain absorption coefficient data appropriate for use in making surface photovoltage (SPV) measurements on specimens with varying amounts of heat treatment, optical transmission measurements are underway. The wavelength range used for SPV measurements in silicon is from about 0.8 to 1.1 μm, in the vicinity of the band gap absorption edge. In this range the absorption coefficient changes rapidly from a value of about 1000 cm^{-1} at 0.8 μm to about 10 cm^{-1} at 1.1 μm. A very thin specimen is needed to obtain accurate transmission measurements when the absorption coefficient is high, and thicker ones are required at wavelengths with less absorption. To cover the wavelength range, four chem-mechanically polished

silicon wafers were prepared with thicknesses of about 30, 100, 300, and 1000 μm. Measurements have been made on the wafers and they have been heat treated at a temperature and time used for a gold diffusion in preparation for the second set of measurements. (M. Cosman, W. R. Thurber, and R. Forman*)

Plans: Several cryostats and associated apparatus will be constructed to facilitate the study of thermally stimulated properties. One of these will be a relatively simple system suitable for use in a production environment. Analysis of the OCVD method will continue with emphasis on efforts to develop quantitative relationships for the short base case. The second set of optical transmission measurements will be made on the heat treated silicon wafers to obtain absorption coefficient data for use in the analysis of SPV measurements.

3.3. GOLD-DOPED SILICON

Objective: To characterize *n*- and *p*-type gold doped silicon in order to develop an energy level model to predict the resistivity of silicon as a function of gold density and to provide inputs for a lifetime model.

Progress: The activation energy of the gold acceptor in silicon was obtained from measurements of the Hall coefficient as a function of temperature on a phosphorus-doped specimen with an initial resistivity of 75 Ω·cm. Gold was diffused at 850°C for 304 h; then both sides of the wafer were lapped to a depth of 125 μm to remove excess surface gold before ultrasonically cutting a Hall bar for the electrical measurements. The room temperature resistivity after gold diffusion was 5.6×10^4 Ω·cm. A gold density of 3.6×10^{14} cm^{-3} was determined by neutron activation analysis on a specimen from the same wafer as the Hall bar.†

The activation energy of the gold acceptor was computed from the data shown in figure 2 by means of a least squares analysis [1] for the slope. The data points included in the analysis are shown by circles; the points excluded because of their deviation from linearity are shown as squares. The calculated energy of 0.5373 ± 0.0003 eV represents the value of the energy difference between the conduction band edge and the gold acceptor level linearly extrapolated from the temperature of the measurements to zero kelvin. The uncertainty in the energy is the square root of the estimated variance of the slope and does not take into account systematic errors which might be present [2]. (W. R. Thurber and M. G. Buehler)

*NBS Solid-State Materials Section.

†The activation analysis was performed by T. Gills of the NBS Activation Analysis Section.

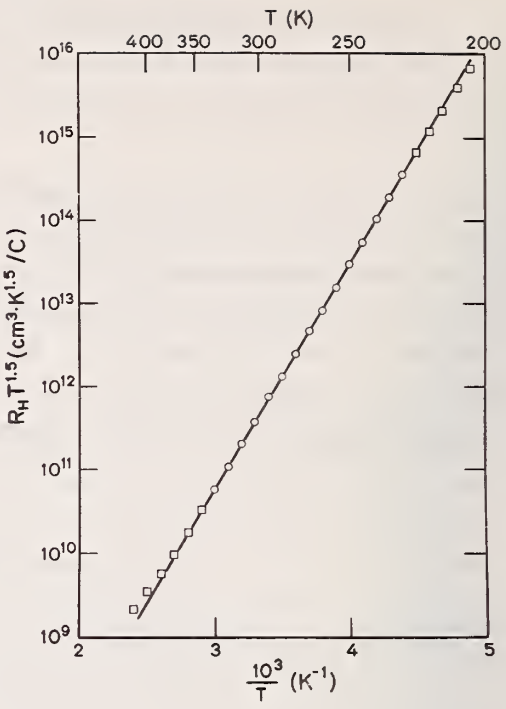

Figure 2. Hall effect activation energy plot for the gold acceptor in *n*-type silicon.

Spreading resistance measurements were made on a boron-doped, gold-diffused silicon wafer to determine the uniformity of the gold diffusion as a function of depth. The resistivity of the wafer after gold diffusion was 2 Ω·cm, twice the initial resistivity. The spreading resistance data which were obtained on an angle lapped region of the specimen showed a constant resistance in the center region with the expected increase in resistance due to excess gold at depths up to 15 to 20 μm from the surface. (P. M. Sandow, W. R. Thurber, and M. G. Buehler)

Plans: Additional Hall effect and resistivity measurements will be made as a function of temperature to obtain additional data on the energy levels of gold in silicon. The resistivity of 0.3- and 1.0-Ω·cm phosphorus-doped wafers, diffused with gold, will be correlated with gold density determined by activation analysis. Spreading resistance measurements will be made on a phosphorus-doped, gold-diffused silicon wafer to study the lateral and depth uniformity of the gold diffusion.

3.4. INFRARED METHODS

Objective: To study infrared methods for detecting and counting impurity and defect centers in semiconductors and, in particular, to evaluate the suitability of the infrared response technique for this purpose.

Progress: Infrared response measurements (IRR) on the 85 germanium specimens collected for the germanium study were completed. The tentative determination of the position within the forbidden energy gap of energy levels detected by IRR in germanium and silicon has been accomplished. The results are in very good agreement with summaries reported in the literature of energy levels detected by various methods after radiation or thermal damage.

Infrared Response Measurements on Germanium — Most of the 85 germanium specimens collected over the past five years had been rejected for use in the fabrication of high-quality Ge(Li) detectors. Infrared response spectra from 55 of these specimens were identified as to spectrum type (NBS Tech. Note 733, pp. 17-21); the remaining specimens were of insufficient thickness from which to fabricate diodes, were damaged during processing, or yielded IRR spectra that were too noisy to identify.

(H. E. Dyson and A. H. Sher)

In early IRR measurements, good agreement had been found between energy levels determined from the energies of IRR spectral features and energy levels arising from radiation damage experiments in germanium (NBS Tech. Note 571, pp. 16-18). However, at that time no attempt was made to distinguish whether features seen in IRR measurements were associated with defects in the upper or in the lower half of the forbidden energy gap.

After a review of the literature concerning energy levels resulting from radiation or thermal damage in germanium as measured either by photoconductivity or Hall effect [1-19], an attempt was made to link features in the IRR spectra specifically with energy levels observed in the literature. The results are shown in figure 3. From the data published on fast neutron, proton, gamma ray, fast electron, and thermal damage, the summary of energy levels shown in column B was obtained. The shaded bars indicate the upper and lower energy range of levels for which there was some discrepancy in reported energy but which appeared to arise from the same center. In column A are shown energy levels resulting from IRR measurements of diode NBS-83-3. In this case each energy level appears only once in the scheme; the level was placed at the appropriate energy either below the conduction band edge or above the valence band edge using the levels shown in column B as the basis for comparison. In the majority of cases, a feature observed in the IRR spectrum can be linked uniquely on the basis of energy with a level or band of levels obtained from the summary of the results reported in the literature.

The energy level located 0.18 eV above the valence band (observed at an energy of about 0.54 eV in IRR spectra) is reported to arise specifically from the divacancy-lithium (VVLi) complex and thus should not be observed in lithium-free germanium [17]. Comparison of the IRR spectra obtained from a lithium-drifted diode, NBS-83-3,

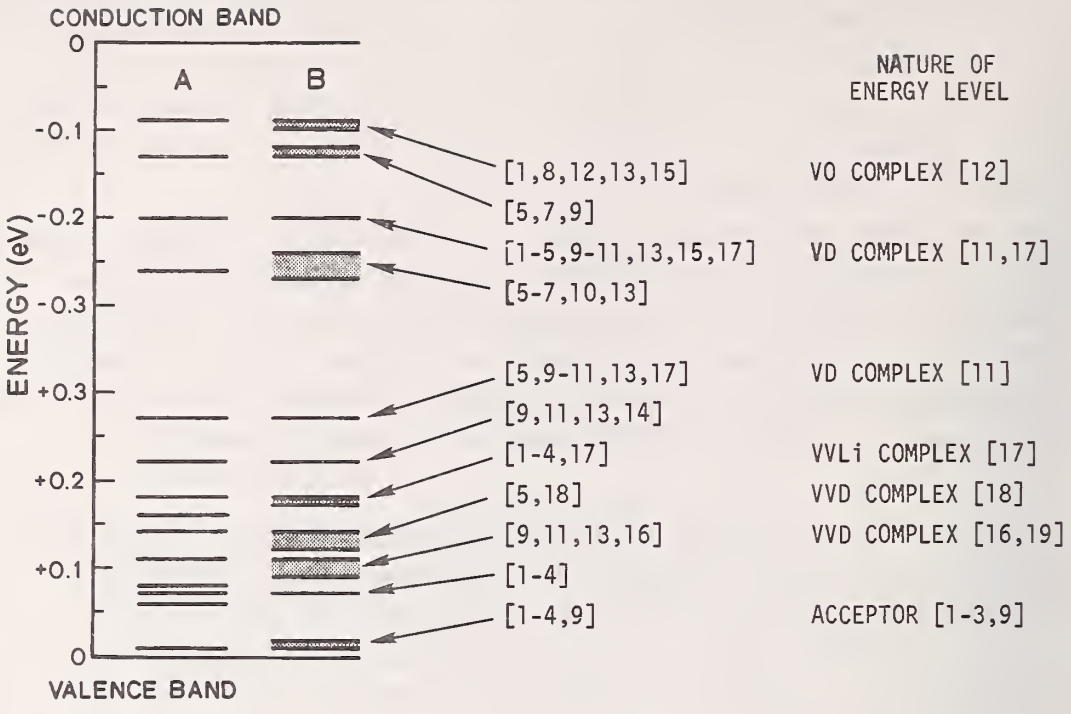

Figure 3. Energy level scheme comparing features detected in IRR measurements on germanium diodes (A) with levels resulting from radiation or thermal damage (B). References are given in brackets. Symbols used: V-vacancy, VV-divacancy, O-oxygen, D-donor, Li-lithium.

and from a diode fabricated from high-purity germanium (without lithium compensation), NBS-112, confirms this expectation (NBS Tech. Note 702, pp. 12-13). The spectrum of NBS-83-3 exhibits a feature at 0.54 eV, but the spectrum of NBS-112 does not.

Infrared Response Measurements on Silicon — The energy level scheme in figure 4 is a summary of the state of the IRR measurements on radiation-damaged, lithium-drifted silicon nuclear radiation detectors. As in the case of germanium, energy levels reported in the literature [20-29] are listed in column B, while energy levels observed in IRR measurements are listed in column A. Tentative identification of IRR-detected levels with corresponding levels reported in the literature has been made previously (NBS Tech. Notes 727 and 733, pp. 18-21 and pp. 20-23, respectively, [30]); however, an attempt to place the levels associated with features in the IRR spectrum in the upper or lower half of the forbidden energy gap had not been made at that time. (A. H. Sher)

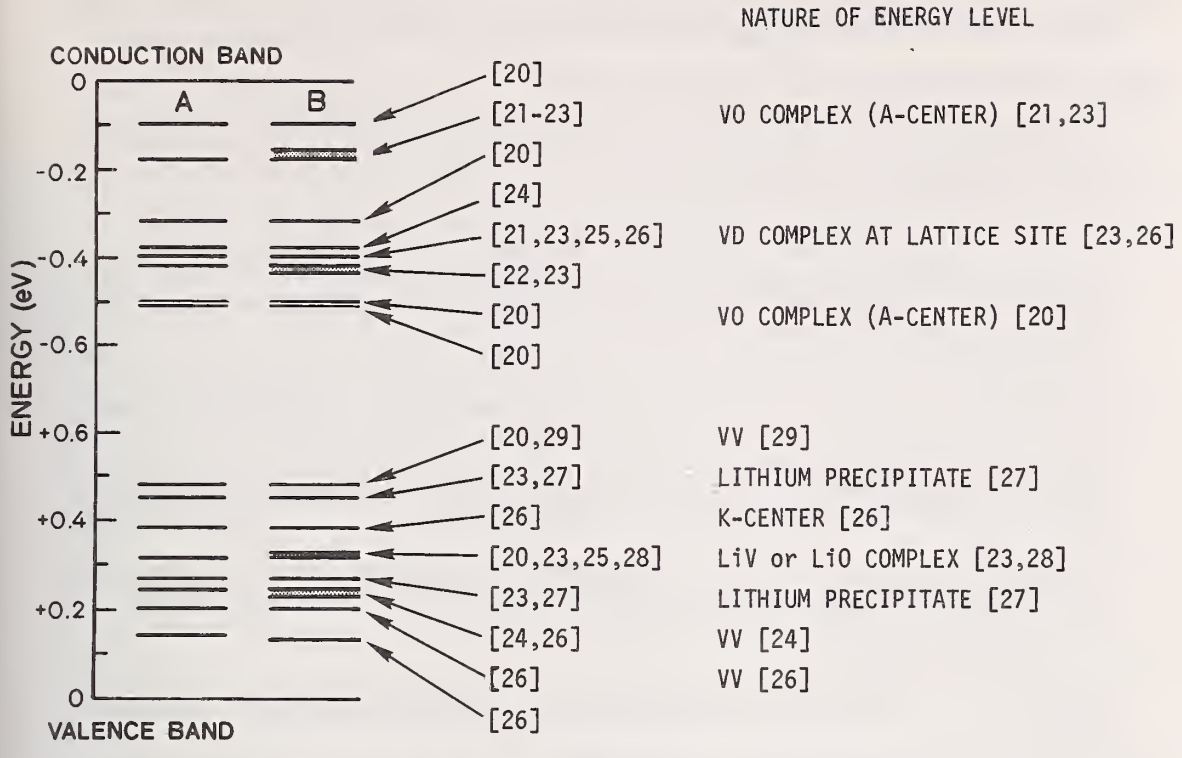

Figure 4. Energy level scheme comparing features detected in IRR measurements on silicon diodes (A) with levels resulting from radiation damage (B). References are given in brackets. Symbols used: V-vacancy, VV-divacancy, O-oxygen, D-donor, Li-lithium.

Plans: The studies of IRR on germanium and silicon diodes will continue. The identification of energy levels and the determination of their effects on detector performance and IRR response will be pursued. Further IRR analysis on silicon devices not compensated with lithium will be resumed.

3.5. REFERENCES

3.1. Resistivity

1. Standard Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array, ASTM Designation F84-72, *Annual Book of ASTM Standards*, Part 8. Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa. 19103.

2. La Chapelle, R., Composition for Polishing Crystalline Silicon and Germanium and Process, U.S. Patent 3,429,080, February 25, 1969.

3. Buehler, M. G., Peripheral and Diffused Layer Effects on Doping Profiles, *IEEE Trans. Electron Devices* ED-19, 1171-1178 (1972).

3.2. Generation-Recombination-Trapping Centers

1. Buehler, M. G., Impurity Centers in *p-n* Junctions Determined from Shifts in the Thermally Stimulated Current and Capacitance Response with Heating Rate, *Solid-State Electronics* 15, 69-79 (1972).

2. Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon *p-n* Junctions, to be published in *Semiconductor Silicon/1973 (Proceedings of the Second International Symposium on Silicon Materials Science and Technology,* Chicago, May, 1973), H. R. Huff and R. R. Burgess, eds. (Electrochemical Society, Princeton, New Jersey, 1973).

3. Lederhandler, S. R., and Giacoletto, L. J., Measurement of Minority Carrier Lifetime and Surface Effects in Junction Devices, *Proc. IRE* 43, 477-483 (1955).

4. Choo, S. C., and Mazur, R. G., Open Circuit Voltage Decay Behavior of Junction Devices, *Solid-State Electronics* 13, 553-564 (1970).

5. Collins, C. B., and Carlson, R. O., Properties of Silicon Doped with Iron or Copper, *Phys. Rev.* 108, 1409-1414 (1957).

3.3. Gold-Doped Silicon

1. Natrella, M. G., *Experimental Statistics,* NBS Handbook 91 (August 1, 1963), ¶5-5.1.3.

2. Thurber, W. R., Lewis, D. C., and Bullis, W. M., Resistivity and Carrier Lifetime in Gold-Doped Silicon, AFCRL Report AFCRL-TR-73-0107, January 31, 1973, pp. 14-24.

3.4. Infrared Methods

1. Konopleva, R. F., Novikov, S. R., and Ryvkin, S. M., High-Temperature Annealing of Defects Produced by Fast Neutrons in Germanium, *Sov. Phys.-Solid State* 6, 2610-2612 (1965).

2. Konopleva, R. F., Novikov, S. R., and Ryvkin, S. M., Energy Levels in Germanium Induced by Fast-Neutron Bombardment, *Sov. Phys.-Solid State* 5, 1345-1351 (1964).

3. Novikov, S. R., Rubinova, E. E., and Ryvkin, S. M., Photoconductivity of Germanium Irradiated with Fast Neutrons, *Sov. Phys.-Solid State* 6, 690-691 (1964).

4. Novikov, S. R., and Rubinova, E. E., Photoconductivity of Germanium Irradiated by Fast Neutrons at 77°K, *Sov. Phys.-Solid State* 6, 1037-1040 (1964).

5. Konopleva, R. F., *et al.,* Radiation Defects in Germanium Irradiated with High-Energy Protons, *Sov. Phys.-Semiconductors* 3, 948-951 (1970).

6. Evseev, V. A., Konopleva, R. F., and Yuferev, A. A., Recombination Properties of *p*- and *n*-Type Germanium Irradiated with 660-MeV Protons, *Sov. Phys.-Semiconductors* 4, 1323-1327 (1971).

7. Evseev, V. A., Konopleva, R. F., and Yuferev, A. A., Investigation of Trapping Phenomena in *p*- and *n*-Type Germanium Irradiated with 660-MeV Protons, *Sov. Phys.-Semiconductors* 5, 625-628 (1971).

8. Vitovskii, N. A., Maksimov, M., and Mashovets, T. V., Investigation of γ-Radiation Defects in High Purity Germanium, *Sov. Phys.-Semiconductors* 4, 880-886 (1970).

9. Vitovskii, N. A., Mashovets, T. V., and Ryvkin, S. M., High Temperature Annealing of γ-Radiation Defects in *n*-Type Germanium, *Sov. Phys.-Solid State* 6, 1481-1487 (1964).

10. Gerasimov, A. B., *et al.*, Impurity Photoconductivity in Germanium Due to Gamma-Ray Irradiation, *Sov. Phys.-Solid State* 6, 2527-2528 (1965).

11. Mashovets, T. V., and Khansevarov, R. Yu., The Energy Structure of γ-Radiation Defects in Germanium, *Sov. Phys.-Solid State* 7, 245-246 (1965).

12. Akimchenkov, I. P., Vavilov, V. S., and Plotnikov, A. F., Photoconductivity Spectra of Germanium Doped with Oxygen and Irradiated with Fast Electrons, *Sov. Phys.-Solid State* 8, 1577-1579 (1967).

13. Gerasimov, A. B., Ryvkin, S. M., and Yaroshetskii, I. D., Impurity Photoconductivity in Germanium Irradiated by Fast Electrons, *Sov. Phys.-Solid State* 6, 543-550 (1964).

14. Akimchenkov, I. P., Ginzburg, M. I., and Plotnikov, A. F., Spectra and Kinetics of the Photoconductivity of *p*- and *n*-Type Germanium Crystals Irradiated with Fast Electrons at 100 and 5.2°K, *Sov. Phys.-Solid State* 8, 932-937 (1966).

15. Tkachev, V. D., and Urenev, V. I., Thermal Defects in Crystals of Pure Germanium, *Sov. Phys.-Semiconductors* 4, 1880-1881 (1971).

16. Abdurakhamonova, S. N., *et al.*, Investigation of Thermal Defects in High-Purity Germanium, *Sov. Phys.-Semiconductors* 4, 1979-1985 (1971).

17. Sinishchuk, I. K., Tkachev, V. K., and Urenev, V. I., Interaction of Lithium with Radiation Defects in Pure *n*-Type Germanium, *Sov. Phys.-Semiconductors* 5, 1910-1911 (1972).

18. Goncharov, L. A., *et al.*, Divacancy Donor Complexes in Oxygen-Free γ-Irradiated Germanium, *Sov. Phys.-Semiconductors* 6, 369-370 (1972).

19. Emtzev, V. V., *et al.*, On the Donor-Vacancy Type Complexes in Germanium, *Rad. Effects* 9, 181-187 (1971).

20. Vorobeichik, V. A., *et al.*, Photoelectric Properties of Si Irradiated with 660-MeV Protons, *Sov. Phys.-Semiconductors* 5, 397-401 (1971).

21. Young, R. C., and Corelli, J. C., Infrared Photoconductivity of Electron-Irradiated Phosphorous Doped Silicon, Air Force Cambridge Research Laboratories Final Report (August 1, 1971); available from NTIS, Springfield, Va. 22151; AD729477.

22. Daley, D. F., and Noffke, H. E., An EPR Study of Fast Neutron Radiation Damage in Silicon, *Rad. Effects* 8, 203-211 (1971).

23. Vavilov, V. S., *Effects of Radiation on Semiconductors*, p. 178 (Consultants Bureau, New York, 1965); contains an energy level scheme compiled from 13 references published up to 1963.

24. Konozenko, I. D., Semenyak, A. K., and Khivrich, V. I., Radiation Defects Created by Co^{60} γ-Rays in *p*- and *n*-Type Silicon of High Purity, *Phys. Stat. Sol.* 35, 1043-1052 (1969).

25. Lappo, M. T., and Tkachev, V. C., Divacancies in Silicon Irradiated with Fast Neutrons, *Sov. Phys.-Semiconductors* 4, 1882-1884 (1971).

26. Johnson, E. S., and Compton, W. D., Recombination Luminescence in Irradiated Silicon — Effects of Thermal Annealing and Lithium Impurity, *Rad. Effects* 9, 89-92 (1971).

27. Smirnova, I. V., Chapnin, V. A., and Vavilov, V. S., Radiation Defects in Lithium-Doped Silicon, *Sov. Phys.-Solid State* 4, 2469-2474 (1963).

28. Urli, N. B., Annealing of γ-Ray Irradiated Lithium Compensated *p*-Type Silicon, *Rad. Effects* 9, 93-97 (1971).

29. Daly, D. F., and Noffke, H. E., The Annealing of Paramagnetic Divacancies in Fast Neutron Irradiated Silicon, *Rad. Effects* 10, 191-195 (1971).

30. Sher, A. H., Liu, Y. M., and Keery, W. J., Infrared Response Measurements on Radiation-Damaged Si(Li) Detector, *IEEE Trans. Nucl. Sci.* NS-19, No. 3, 312-317 (1972).

4. SEMICONDUCTOR PROCESS CONTROL

4.1. DIE ATTACHMENT EVALUATION

Objective: To evaluate methods for detecting poor die attachment in semiconductor devices with initial emphasis on the determination of the applicability of thermal measurements to this problem.

Progress: A tape of the revised TRUMP thermal analysis computer program was received and modifications for its use on the NBS computer were undertaken. Infrared microradiometer measurements on a number of previously investigated diodes with controlled voids indicated that the percent increase in peak junction-to-case temperature difference of diodes with voids over that of their respective controls, measured under steady-state conditions, correlated well with the electrical steady-state thermal response measurements. The infrared measurements also confirmed a previously noted trend that the sensitivity to void sizes of both 20 and 40 percent of the chip bonding area was nearly the same. Measurements of thermal response made on transistor chips with 40 percent void area in the transistor die attachment indicated that there was no advantage, with respect to void sensitivity, of measuring the devices in the diode-connected transistor operating mode over that of the normal transistor operating mode. When the transistors were measured in the transistor operating mode, transient thermal response measurements made with a 5-ms wide heating power pulse were nearly seven times more sensitive to the presence of voids than were the steady-state thermal response measurements.

Analysis — A tape of the revised TRUMP thermal analysis computer program was received from the author [1]. Modifications were undertaken for its use on the NBS computer to develop information regarding the limitations of thermal response techniques for detecting poor die adhesion in diodes. (R. L. Gladhill)

Diodes — A heat sink for use in infrared microradiometer measurements of the previously investigated diodes with controlled voids (NBS Tech. Note 717, pp. 19-22) was fabricated. Peak steady-state, junction-to-case, thermal response measurements using the infrared microradiometer were made on two representative samples from each lot of diodes with 10, 20 and 40 percent void area in the diode die attachment and on two representative control samples (diodes with no intentional voids) from each lot. In table 1 the percent increase in the peak junction-to-case temperature difference, calculated on the basis of the average of the two controls from each lot, is compared with the percent increase in junction-to-case temperature difference previously measured electrically under steady-state conditions. The data indicate that the trend noted previously, in which the percent increase in steady-state thermal response due to the presence of voids was essentially the same for void areas of both

20 and 40 percent, also occurs for the case of peak junction-to-case temperature difference as measured with the infrared microradiometer.

(F. F. Oettinger and D. L. Blackburn)

Transistors — The circuit for electrically measuring the thermal response of *n-p-n* transistors (NBS Tech. Note 743, pp. 23-24) has provisions for use in both diode and transistor operating modes. To compare the two operating modes, measurements of steady-state thermal response and transient thermal response for a 20-ms wide heating-power pulse were made on a group of eight transistors bonded to TO-5 headers. A dimple, 25-mil (0.64-mm) in diameter, had been ultrasonically machined into the bonding surface of each header to provide a void that is approximately 40 percent of the total chip bonding area. Nine control devices without voids were also measured. The transistor chips were 35-mil (0.89-mm) square.

The results of the measurements are summarized in the first two columns of data in table 2.* The first group of entries gives the junction-to-case temperature difference measured under steady-state conditions for the control transistors [ΔT_{ss} (controls)] and the transistors with voids [ΔT_{ss} (voids)]. The heating current and voltage for the transistor mode were I_C = 50 mA and V_{CE} = 10 V, respectively, while for the diode mode, the heating current was 300 mA. The third line is the increase in the average junction-to-case temperature difference of the voided devices over that of their controls expressed as a percentage of the latter. The range given is one sample standard deviation. The second group of entries gives the junction-to-case temperature measured 10 μs after the termination of the 20-ms power pulse for the control transistors [ΔT_t (controls)] and the transistors with voids [ΔT_t (voids)]. The heating current and voltage for the transistor mode were I_C = 150 mA and V_{CE} = 10 V, respectively, while for the diode mode, the heating current was 800 mA. The third line of this group is the increase in the average junction-to-case temperature difference of the voided devices over that of their controls expressed as a percentage of the latter. Again, the range given is one sample standard deviation. The last line of the table gives the ratio of the average percent increase obtained for transient response measurements to that obtained for steady-state response measurements. This quantity is indicative of the increase in sensitivity to voids of transient response over that of steady-state response. Because the entries in the table have been rounded, the numbers may not check exactly.

These results indicate that although there is no appreciable difference in the sensitivity to voids between the two modes of transistor operation, there is

*Data in the last column of table 2 were obtained in a subsequent experiment and will be discussed below.

Table 1 — Percent Increase in Average and Peak Steady-State Junction-to-Case Temperature Difference of Diodes with Controlled Voids over Diodes Without Voids

Device Number	Percent Void Area	Percent Increase (Average)[a]	Percent Increase (Peak)[b]	Ratio[c]
JV-9	10	-0.5	0.	0
JV-10	10	+4.1	0.	0
LV-6	20	+7.2	+14.3	2.0
LV-8	20	+6.8	+14.3	2.1
IV-10	40	+8.1	+14.3	1.8
IV-12	40	+10.3	+21.4	2.1

[a] Increase with respect to all control diodes without voids in the lot; average junction temperature determined electrically.

[b] Increase with respect to two control diodes without voids from each lot; peak junction temperature determined with infrared microradiometer.

[c] Ratio of peak to average percent increase.

Table 2 — Summary of Results of Junction-to-Case Temperature Difference Measurements on Lot AT Transistors

Steady State Measurements			
Operating Mode	Transistor	Diode	Transistor
ΔT_{ss} (controls), °C	30.3±0.6	14.8±0.5	30.5±0.5
ΔT_{ss} (voids), °C	32.6±0.6	15.8±0.6	32.2±0.5
% increase, ss	8±3	8±6	6±2
Transient Measurements			
Operating Mode	Transistor	Diode	Transistor
Heating Power Pulse Width	20 ms	20 ms	5 ms
ΔT_t (controls), °C	33.1±1.0	17.0±1.2	21.7±0.5
ΔT_t (voids), °C	42.5±1.6	21.1±1.2	29.8±1.2
% increase, t	28±6	24±10	37±6
Ratio			
$\frac{\%\text{ increase, t}}{\%\text{ increase, ss}}$	3.7	3.6	6.7

a distinct advantage in using the transistor operating mode for use in screening transistors for poor die adhesion. The spread in junction-to-case temperature difference is essentially independent of the magnitude; since larger differences are obtained in the transistor operating mode, the spread is a smaller percentage of the value. Further, in the diode operating mode, the heating current levels needed to give reproducible junction-to-case temperature differences for the heating power pulse width required for maximum sensitivity to voids may not always be obtainable due to the current handling limitations of the transistor under test. It was therefore decided to perform no further studies on transistors operated in the diode-connected mode.

Measurements of steady-state thermal response and transient thermal response for heating-power pulse widths ranging from 2 to 100 ms were made on nine transistors with and nine transistors without voids from the same group. The transistor operating conditions were the same as those used for the transistor operating mode in the previous measurements. The results indicated that a 5-ms heating power pulse gave the maximum sensitivity; results of the measurements made with this pulse width are given in the last column of table 2. (F. F. Oettinger and R. L. Gladhill)

Plans: The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in the diodes previously investigated will resume after the revised TRUMP thermal analysis program is suitably modified for use on the NBS computer. The initial series of measurements of steady-state and transient thermal response on transistors will be completed with the measurements of transistors with controlled voids that are approximately 15 and 25 percent of the total chip bonding area. Long-term, single-operator measurements of steady-state and transient thermal response will be undertaken to check the reproducibility of the transistor die attachment evaluation equipment.

4.2. WIRE BOND EVALUATION

Objective: To survey and evaluate methods for characterizing wire bond systems in semiconductor devices and, where necessary, to improve existing methods or develop new methods in order to detect more reliably those bonds which will eventually fail.

Progress: Further measurements of pull strength as a function of loop height for two-level bonds indicate that the variability in the experimental results observed to date may be due to substrate fabrication problems. Analysis of results on annealed single-level wire bonds indicates that elongation of the wire during pulling and subsequent increase in bond loop height probably accounts for the observed

differences between experiment and theory. The report summarizing the work on ribbon wire has been completed and is being reviewed prior to publication.

Deposition Rate of Bonding Pad Metallization — An evaporation-rate monitor that completes the electron-beam vacuum deposition system was put into service. Since this systems affords a greater degree of control over deposition rate than was heretofore available, an experiment was performed to determine how bonding pads produced by various deposition rates of aluminum affect the measured pull strength of bonds made on these pads. Four bonding pad substrates were prepared in the usual manner (NBS Tech. Note 527, pp. 39-41) except that aluminum was deposited on the cold oxide-coated silicon wafers at a rate of 1.5, 5, 10, or 20 nm/s. On each substrate, groups of 10 single-level bonds (0.3-mm loop height, 1-mm bond-to-bond spacing) were made at each of 8 to 10 power settings. The range of power settings was such that groups of bonds resulted that lifted off the pads at the lowest power and were adherent but highly deformed at the highest power. The results from each of the four substrates plotted as pull strength as a function of ultrasonic power were similar to other power series curves previously reported (NBS Tech. Note 560, pp. 30-33). The average pull strength for bonds made on the film deposited at 20 nm/s was about 20 percent greater than that for film deposited at 1.5 nm/s, but the standard deviation was found to be approximately twice as great for the highest deposition rate as compared to the lowest. A rate of 5 nm/s was selected to yield an optimum combination of high strength and low variability. Since this rate is close to the rate used to prepare the substrates used in previous investigations; no problem in relating subsequent results to previous ones is anticipated.

(K. O. Leedy and J. Krawczyk)

Pull Test Evaluation — Measurements of pull strength as a function of bond loop height for two-level bonds were repeated. Previous results (NBS Tech. Note 754, pp. 21-23) indicated that for bond pairs made with the first bond to the high pad there appeared to be agreement between the trend of the experimental points and the theoretical curve, while such agreement was not evident when the first bond was made to the low pad. Experimental results duplicating the initial set agreed with theory for both cases over a loop height range of from about 0.02 to 0.3 mm. That the previous measurements where the first bond was made to the low pad are not in agreement with the present results would seem to indicate that some unknown factor is contributing to the inconsistency in test results. (K. O. Leedy and C. A. Main)

One possible source of variability in the two-level system appears to be the manner in which the substrates are constructed. Problems were often encountered during the quarter in producing suitable substrates. The step is formed by gluing a strip of silicon directly to a substrate that itself has bonding pads patterned

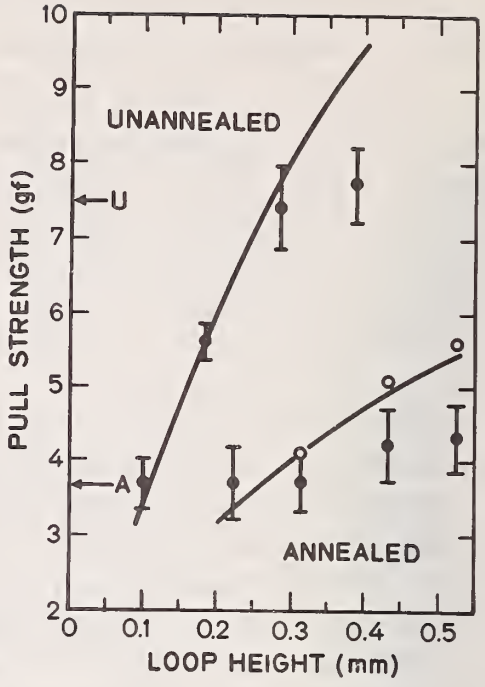

Figure 5. Pull strength of unannealed round-wire bonds (upper left) and annealed round-wire bonds (lower right) as a function of loop height. (Each solid data point represents the mean for a group of 10 bonds, the error bar represents one sample standard deviation. See text for a discussion of the open data points. The solid curves are calculated from resolution of forces using the wire tensile strength indicated by the arrows: U - unannealed, A - annealed).

onto it (NBS Tech. Note 754, pp. 21-22). It is conceivable that uniform contact is not being obtained across the length of the silicon strip. An alternative procedure in which two silicon strips are glued to a metal plate with a milled step is under investigation. (G. G. Harman)

A series of experiments was performed in a further effort to determine the reason agreement had not been obtained between the pull strength variation with loop height of annealed single-level bonds and the theoretical prediction (NBS Tech. Note 743, pp. 29-31). On a single substrate, groups of bond pairs were made at four loop heights with a nominal bond-to-bond spacing of 40 mils (1 mm). About half of these bonds were pulled to breaking in groups of ten at five different rates of pull. The remaining bonds were annealed at 505°C for 25 min and then groups of ten were pulled at each of the five rates. In agreement with previous measurements, the unannealed bonds did not exhibit any dependence of pull strength on rate of pull. Although there is an indication that the annealed bonds show some dependence of pull strength on rate of pull, certain apparently anomalous results need further resolution.

However, it appears that the main reason the experimentally determined pull strength dependence of annealed bonds on loop height did not agree with theory lies in the fact that annealed wire undergoes considerable elongation during pulling. The loop heights of annealed bonds at bond rupture are substantially larger than they are in the original unannealed state. In figure 5, pull strength is shown as a function

of loop height for the unannealed and annealed bonds studied. The differences in loop height between the annealed bonds and the unannealed state at which all bonds were made is evident. As before, the agreement with experimental data for unannealed bonds of the solid curve predicted by the resolution of forces analysis (NBS Tech. Note 555, pp. 31-36) is acceptable up to a loop height that corresponds to an h/d ratio of about ¼. No such agreement could be obtained for the data (solid points) obtained from annealed bonds. However, it can be seen that most of these points are for loops whose values are greater than the point where agreement between experiment and theory had been obtained for unannealed bonds. This lack of agreement has been attributed to the weakening effect of bond peel at large loop heights (NBS Tech. Note 743, pp. 29-30).

From the unannealed bond data, the percentage increase in pull strength required to bring the grand average of all pull strength group means at each loop height to coincidence with the theoretical curve was calculated. A linear relationship was obtained between percent correction in pull strength against measured pull strength. This was extrapolated to the larger loop height values appropriate to the annealed bonds. When the annealed bond data were corrected using this curve, the open points shown in figure 6 were obtained. It can be seen that these points appear to be in reasonable agreement with the theoretical curve shown. (A. H. Sher and C. A. Main)

Plans: The experimental study of the pull test on two-level substrates will be completed unless further technical problems are encountered with substrate fabrication.

4.3. REFERENCE

4.1. Die Attachment Evaluation

1. Edwards, A. L., TRUMP: A Computer Program for Transient and Steady-State Temperature Distributions in Multidimensional Systems, Lawrence Radiation Laboratory, Univ. of California, Livermore, California, UCRL-14754, Rev. II, 1 July 1969. Available from the National Technical Information Service, Springfield, Virginia 22151.

5. SEMICONDUCTOR DEVICES

5.1. THERMAL PROPERTIES OF DEVICES

Objective: To evaluate and improve electrical measurement techniques for determining the thermal characteristics of semiconductor devices.

Progress: Measurements of peak junction temperature were made with an infrared microradiometer on a group of transistors on which thermal resistance had been previously measured by both the emitter-only and the emitter-and-collector switching techniques. In both cases the measurements were made under conditions such that there were no severe current constrictions or hot spots. In most cases, the junction-to-case thermal resistance calculated from electrical measurements by the emitter-only switching technique extrapolated to 1 μs after the termination of the heating power pulse was within 10 percent of that determined from the infrared measurement. Further investigations were made into the mechanism of the emitter-base voltage and current transients which occur when switching the emitter with a series transistor during the measurement of thermal resistance by the emitter-only switching technique.

Standardization Activities — The first draft of a proposed revision of Method 1012, Thermal Characteristics, of MIL-STD-883, Test Methods for Microcircuits, undertaken at the request of the cognizant agency, was completed. (F. F. Oettinger)

Thermal Resistance Methods — The tests to provide a broader basis for conclusions regarding the superiority of the emitter-only switching technique for measuring thermal resistance were continued. Tests reported previously (NBS Tech. Note 754, pp. 25-27) indicated that the emitter-only switching method of thermal resistance measurement consistantly yields a value indicative of a higher apparent junction temperature than that yielded by the collector-and-emitter switching method for the same delay time after the cessation of the power pulse. Infrared measurements of thermal resistance were made on 16 of the 18 originally tested transistors. The devices not included failed prior to being measured with the infrared microradiometer. In preparation for the infrared measurements each chip was coated with black paint approximately 15 μm thick. Then each chip was scanned manually for the hottest part during operation, the temperature of which was then measured and the thermal resistance calculated from the temperature rise. Test conditions for the measurements on the TO-66 encased transistors were generally such that severe current constrictions or hot spots did not occur. Consequently, measurements were made under high-current, low-voltage conditions. All devices were measured with a collector-emitter voltage of 20 V and a case temperature of 25°C. The collector current was held at 1 A; except in the case of two low-gain devices for which the collector current was 0.5 A. The results are shown in column 2, labeled $R_{\theta JC}$(IR) of table 3.

Table 3 — Comparison of Infrared and Electrical Thermal Resistance Measurements

Device	$R_{\theta JC}$ (IR), °C/W	A, %	B, %	C, %
1	6.14	-16.4	-11.7	-3.3
2	5.90	-14.9	-10.8	-3.2
3	2.85	-21.1	-16.5	-6.7
4	3.36	-31.0	-25.3	-14.3
5	3.39	-13.3	-----[b]	-2.7
6	5.24	-12.4	-8.0	-0.6
7	3.55	-31.5	-24.5	-9.3
8	7.49	-15.8	-12.0	-4.8
9	3.48	-17.8	-----[b]	-10.9
10	3.65	-33.7	-24.7	-6.0
11	3.36	-29.2	-21.4	-6.0
12	2.94	-32.7	-24.1	-6.5
13	3.33	-14.7	-10.2	-3.6
14	3.14	-10.5	-6.7	-1.0
15[a]	7.40	-5.7	-1.5	+5.7
16[a]	7.13	-2.4	+3.2	+11.6

a For devices 15 and 16: I_C = 0.5 A.

b Measurement not made because of interferences of long electrical transients.

Steady-state thermal response measurements were also made electrically by the emitter-only switching method. The emitter-base voltage was measured 5, 10, 20, 50, and 100 μs after the end of the power cycle, with a test current of 6.5 mA. The differences between the thermal resistance calculated from the junction temperature determined electrically 50 and 10 μs after the cessation of the power and that determined from the infrared measurements, expressed as a percentage of the latter, are listed in column 3, labeled A, and column 4, labeled B, respectively, of table 3.

The entire set of electrical readings was used to determine the junction temperature 1 μs after the end of the power cycle. The junction temperature cannot be measured directly at this time because of the interference from electrical switching transients. However, it was noted that between 5 and 100 μs the junction-to-case temperature difference, ΔT_{JC}, can be represented to a reasonably good approximation by $\Delta T_{JC} = A(t_{meas})^{-B}$ where A is a constant, t_{meas} is the time between the end of the power cycle and the measurement, and -B is the slope of the curve of log ΔT_{JC} against

log t_{meas}. The temperature was determined by extrapolating the experimentally determined curve of log ΔT_{JC} against log t_{meas} back to 1 μs and the thermal resistance calculated. The difference between this value of thermal resistance and that determined from the infrared measurements expressed as a percentage of the latter is listed in the last column, labeled C, of table 3.

For 14 of the 16 transistors tested, the electrically measured junction temperature was lower than the temperature measured by the infrared microradiometer. For the remaining two transistors the temperature measured by the infrared microradiometer was lower than the temperatures measured with the emitter-only switching technique at t_{meas} = 5 μs. This discrepancy could be accounted for by an inability to measure the hottest area of the transistor chip with the microradiometer either because the hottest area was under one of the leads or because of excessive spreading of the heat before it reached the chip surface. Although the log-log extrapolation technique appears to offer a significant improvement in deriving from electrical measurements the temperature of the hottest region of the transistor chip, it was generally observed that as the uniformity of the current distribution is decreased and hot spots become more prominent, the difference between the electrically determined thermal resistance and that calculated from the infrared measurement increases.

(S. Rubin, D. L. Blackburn, and F. F. Oettinger)

It was reported previously (NBS Tech. Note 754, p. 27) that the process of rapidly reducing the emitter current from a very high value during heating to a very low value during measurement while the collector remained connected to its voltage supply resulted in an apparent reverse-bias breakdown of the emitter-base junction of some transistors. Since the transistor may be damaged [1] by reverse-biased breakdown of the emitter-base junction, fast switching circuits such as those needed for measurement of thermal resistance must be designed to avoid the possibility of such breakdown. The mechanism for this breakdown and the operation of a protective circuit were studied extensively during the present period. It appears that the excess majority carriers in leaving the active region of the base through the base contact cause a lateral current in the base and a potential drop along the base side of the emitter-base junction. Since the emitter side of this junction is essentially an equipotential which floats with the central portion of the active base region under the conditions encountered in these devices, a potential difference is built up across the emitter-base junction. In the central region the voltage across the junction is in the forward direction and rather small. At the periphery, however, the voltage drop is in the reverse direction; its magnitude is determined by the voltage applied between the collector and the base. If the voltage drop reaches the reverse-bias breakdown voltage of the emitter-base junction, breakdown occurs and further significant increases in the voltage drop do not occur. The protective circuit described

previously (NBS Tech. Note 754, p. 27) acts to limit the potential drop across the emitter-base junction to values lower than the breakdown voltage. (S. Rubin)

Plans: On completion of the interlaboratory testing, the results of the round-robin experiment on thermal resistance measurements being conducted in cooperation with JEDEC Committee JC-25 on Power Transistors will be summarized. The final draft of the proposed revision of Method 1012, Thermal Characteristics, of MIL-STD-883, Test Method for Microcircuits, will be written and sent to the cognizant agency. Long-term, single-operator measurements will be undertaken to check the reproducibility of the equipment for measuring thermal resistance of transistors by the emitter-only switching technique. Thermal resistance measurements will be made under non-uniform current distribution operating conditions by the emitter-only switching technique on a number of the transistors measured this quarter. The results will be compared with thermal resistance derived from measurements of peak junction temperature made with the infrared microradiometer. Additional investigations of the switching transients encountered when measuring thermal resistance on some devices will be completed and a detailed description of the mechanism of emitter-base junction breakdown will be prepared.

5.2. MICROWAVE DEVICE MEASUREMENTS

Objective: To study the problems and uncertainties associated with the measurement of electrical properties of microwave diodes, and to improve the techniques of these measurements.

Progress: Additional sensitivity relations were developed to estimate systematic measurement uncertainty. The basic conversion loss equation for the voltage form of the incremental modulation method is (NBS Tech. Note 754, pp. 30-31)*

$$L_M = 8m^2\ PRM/V^2 \qquad (8)$$

where L_M is the conversion loss (power ratio), m is the modulation factor (voltage ratio), P is the unmodulated local oscillator power (watts) available to the mixer, R is the incremental (i-f) load resistance (ohms), V is the incremental (i-f) load voltage (volts), and M is the i-f mismatch factor (power ratio). Only that portion of the dependence of L_M on P which results from sensitivity to the r-f signal is included in eq (8). The r-f signal, which is produced by modulating the local oscillator, is directly proportional to the local oscillator power since the modulation

*Note that the i-f mismatch factor in the previous report is the inverse of that used in the present work.

factor is fixed. The sensitivity of conversion loss, expressed in decibels ($L_M' = 10 \log L_M$), to variations in local oscillator power as reflected in r-f signal variations is

$$\frac{\partial L_M'}{\partial P} = \frac{4.34}{P} \text{ dB/W.} \tag{9}$$

At the nominal power level of 1 mW used in the present test system the sensitivity is 0.00434 dB/μW. This constitutes most of the empirically determined total sensitivity of conversion loss to local oscillator power variations (NBS Tech. Note 743, p. 38). The remainder results from a direct dependence of conversion loss on local oscillator power. That this portion, which depends on individual mixer diode characteristics is about an order of magnitude lower than the diode-independent contribution from eq (9) confirms the observed lack of variation in the measured total sensitivity from diode to diode.

Similar expressions can be obtained for the sensitivity of the conversion loss to variations in i-f load resistance and i-f load voltage. At the levels of these quantities used in the present test system, these sensitivities, when multiplied by the uncertainties in the quantities involved, make only minor contributions to the overall systematic uncertainty in conversion loss as compared with the contributions made by the sensitivities to modulator attenuation and to local oscillator power.

(J. M. Kenney)

To assess repairs made to the modulation attenuator, it was operated repeatedly while observations were made of the variations in voltage output from a calorimeter used to monitor the power level. Since the sensitivity of power to vane rotation is very low at the 0-dB stop used for the modulation crest, the power was readjusted at this stop to obtain a common reference for each cycle. The attenuator was then turned either to the 0.486-dB stop used to set the unmodulated local oscillator power or to the 1-dB stop used for the modulation trough and the calorimeter voltage was recorded. Prior to readjusting the power for the next cycle, the attenuator was returned to the 0-dB stop and the calorimeter voltage was again recorded.

Comparison of the voltage variation at the 0.486-dB or 1-dB stop with that at the 0-dB stop indicated that the variability of attenuator setting was not responsible for most of the power variation. The total conversion loss measurement uncertainty (3 standard deviations) due to power variations (from whatever cause) at the three stops was estimated to be about ±0.11 dB. This is greater than was actually obtained for most diode measurement runs prior to the attenuator repair (NBS Tech. Note 754, pp. 29-30). Calorimeter voltage measurements similar to those reported above, made prior to final attenuator bearing adjustments, yielded sample standard deviations

considerably lower. Additional measurements are being made to resolve these differences. (F. H. Brewer, V. Boxwell, and J. M. Kenney)

Standardization Activities — Definitions of mixer terms were distributed to members of the mixer and detector task group of the IEEE-GED Standards Committee for Electron Devices. Based upon their replies, revised definitions were sent to the IEC TC-47 Technical Advisor as suggested replacements for definitions in document 47(Central Office)430 and as revisions for the definitions previously sent.

(J. M. Kenney)

Plans: The technical report of progress to date, begun last quarter, will be edited and revised, and the illustrations prepared. The report will cover all aspects of the measurements made with a low intermediate frequency (audio and incremental d-c), principally of conversion loss, but also including i-f conductance and r-f reflection measurements. The uncertainty studies will be continued, and the modulation attenuator and bolometers will be recalibrated after the attenuator stability seems assured.

5.3. CARRIER TRANSPORT IN JUNCTION DEVICES

Objective: To improve methods of measurement for charge carrier transport and related properties of junction semiconductor devices.

Progress: The S-parameters of three of the six special high-frequency probe assemblies for electrical probing of transistors at the wafer stage were measured over the frequency range 0.2 to 2 GHz. The upper limit of transistor delay-time error caused by inductance in the collector-base circuit of the vector voltmeter apparatus was computed. Five of the participants in the interlaboratory test of S-parameter measurements completed their transistor and passive network measurements; the sixth completed the passive networks and is beginning the transistor measurements.

Measurement of High-Frequency Transistor Parameters at the Wafer Level — Three of the six transistor special high-frequency probe assemblies (NBS Tech. Note 743, pp. 40-41) were measured with an automatic network analyzer from 0.2 to 2.0 GHz at 100 MHz intervals to yield the S-parameters characterizing the assemblies. The results allow the sponsor to determine the effects of the probes on transistor high-frequency measurements. The measurements employed one of the probe reference unit wafers (NBS Tech. Note 754, pp. 32-33) in the work station designed to manipulate the wafer relative to a probe assembly (NBS Tech. Note 743, pp. 41-42).

(R. L. Jesch*)

*NBS Electromagnetics Division

Vector-Voltmeter Delay-Time Instrumentation — An estimate of the upper limit of delay-time errors ascribable to inductance in the collector-base circuit of the vector voltmeter apparatus may be calculated for any device of known equivalent circuit in the transistor socket. For the bipolar transistor equivalent circuit employed (NBS Tech. Note 717, pp. 37-38), interpretation of the analysis previously completed (NBS Tech. Note 727, pp. 59-61) shows that the error contribution is $\tau_c/[(f_o/f)^2 - 1]$ where τ_c is the product of r_b, the extrinsic base resistance of the transistor, and C_c, the transition region capacitance of the collector-base junction, and f_o is the frequency at which L_t, the inductance between the collector and base pins in the transistor test fixture, resonates with C_c. It is apparent that although the error increases as f approaches f_o, it may be negligible for a low-power, high-frequency device. For example, for a device with r_b = 30 Ω and C_c = 10 pF in an apparatus with L_t = 45.5 nH (NBS Tech. Note 754, pp. 33-35), τ_c = 300 ps and f_o = 235 MHz. At 30 MHz, the design upper operating frequency, the delay time error is 5 ps, which is approximately the resolution limit of the apparatus.

(D. E. Sawyer and G. J. Rogers)

Interlaboratory Comparison of S-Parameter Measurements — During the quarter, five participants in the interlaboratory comparison of S-parameter measurements (NBS Tech. Note 743, pp. 42-43) completed their measurements on the transistors and passive devices; the sixth completed his measurements on the passive devices and has begun the transistor measurements.

Each of the participants who has completed his measurements has furnished NBS with punched paper tapes containing the following data:

1. four sets of measurements on a pair of 10-dB coaxial attenuators connected in series,
2. four sets of measurements on each of three R-C networks in a transistor fixture furnished by NBS,
3. four sets of measurements on each of three R-C networks in the participant's transistor fixture, and
4. one set of measurements on each of 18 *n-p-n* silicon transistors (six each of types 2N709, 2N918, and 2N3960) at seven biases.

All transistor measurements were made at a collector-emitter voltage of 5 V. Most participants took data at emitter currents of 1.6, 2.0, 2.5, 4.0, 5.0, 8.0, and 10.0 mA; to shorten the time required, one participant measured at every other emitter current value and omitted measurements on three each of two of the three types of transistors. The passive elements were measured over the frequency range from 0.2 to 2 GHz in 100 MHz increments. Type 2N709 and 2N918 transistors were measured from 0.2 to 1 GHz in 100 MHz increments, and type 2N3960 transistors, from

Table 4 — Comparison of Reference Planes Used During Calibration Procedures

Step	Specified Load	20-dB Attenuator	Transistors and R-C Networks				
			Lab 1	Lab 2	Lab 3	Lab 4	Lab 5
1, 2	50 Ω at input and output	Output ports	Transistor socket	Output ports	Output ports	Output ports	Thru line at transistor socket[h]
3	50 Ω at both terminals[a]	Output ports[b]	Transistor socket	Transistor socket	Transistor socket	Output ports	Transistor socket
4, 5	Short at input and output	Output ports	Transistor socket	Transistor socket	Output ports	Output ports	Transistor socket
6, 7	Open at input and output	Output ports	Transistor socket	Transistor socket	Output ports	Output ports	Not measured[i]
	(Capacitance)	0.21 pF[c]	-0.6 pF[c]	-0.195 pF[f]	0.21 pF[c]	0.21 pF[c]	
8	Through line	Output ports	Transistor socket	Transistor socket	Transistor socket	Transistor socket	Transistor socket
	(Length)	46.525 cm[d]	0.1 cm[e]	0.1 cm[e]	49.05 cm[g]	49.05 cm[g]	0.1 cm[e]

a Terminals left open when calibrating at transistor socket

b One participant left terminals open when making this measurement

c Specified by manufacturer of test equipment

d Through line and length furnished by NBS

e Length of through line for TO-18 socket (specified by manufacturer)

f Empirically determined by participant

g Total length of transistor fixture with through line

h Measuring equipment "sees" 50 Ω load connected to output terminals of test socket

i Not measured because at least 10-dB of isolation provided between output ports and transistor socket

0.2 to 1.8 GHz in 100 MHz increments. To establish the stability of the transistor characteristics, the S-parameters of each transistor were measured on the same system before and twice during the interlaboratory experiment.

The measurement systems used by the participants in the interlaboratory experiment are calibrated by measuring loads of known characteristics to determine correction factors for the elimination of errors caused by mismatch, directivity, cross-talk, and frequency response. The loads employed for this purpose are a 50-Ω termination, a through line between input and output, an open circuit, and a short circuit. Since these loads must be connected at the measurement reference plane, two sets of calibration standards are required, one for calibration at the output ports of the network analyzer when the device to be measured is equipped with coaxial connectors, and one for calibration at the transistor socket when the device to be measured plugs into a transistor socket.

The coaxial attenuators were measured at the output ports of the measurement system. Each participant had a complete set of standards for calibration at these terminals; NBS furnished a rigid through line to eliminate errors which might have been caused by rotating joints if each participant had used his own through line. Only one participant had a complete set of standards for calibration at the transistor socket. The others lacked a 50-Ω termination that would fit a TO-18 socket. To compensate for this, parts of the calibration were performed at the output ports, with the transistor fixture removed. No two participants performed the calibration in exactly the same way; reference planes and associated conditions used during calibration are listed in table 4. The data from the measurement of the coaxial attenuators and from the measurement of the R-C networks in the NBS transistor fixture are being analyzed to determine if there is a significant difference caused by these variations in procedure. (G. J. Rogers, F. H. Brewer, V. A. Cevrain, and F. R. Kelly)

Plans: The evaluation of the high-frequency probe assemblies and characterization of the Sandia bridge and vector voltmeter systems for measuring transistor delay time will be completed. Analysis of the data taken on the passive elements in the interlaboratory experiment will be completed, and analysis of the data taken on transistors will begin.

5.4. REFERENCE

5.1. Thermal Properties of Devices

1. Verway, J. F., On the Mechanism of h_{FE} Degradation by Emitter-Base Reverse Current Stress, *Microelectronics and Reliability* 9, 425-432 (1970).

APPENDIX A
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APPENDIX B
COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

W. M. Bullis, Editor, Subcommittee 4, Semiconductor Crystals; Secretary, Subcommittee 91, Editorial; Leaks, Resistivity, Mobility, Dielectrics, and Compound Semiconductors Sections; Subcommittee 11, Quality and Hardness Assurance; Advisory Committee

J. R. Ehrstein, Chairman, Resistivity Section; Epitaxial Resistivity, and Epitaxial Thickness Sections

J. C. French, Chairman, Subcommittee 91, Editorial; Subcommittee 11, Quality and Hardness Assurance; Secretary, Advisory Committee

G. G. Harman, Secretary, Interconnection Bonding Section

B. S. Hope, Committee Assistant Secretary

K. O. Leedy, Chairman, Interconnection Bonding Section

T. F. Leedy, Photoresist and Dielectrics Sections

D. C. Lewis, Subcommittee 11, Quality and Hardness Assurance

C. P. Marsden, Committee Secretary; Advisory Committee

R. L. Mattis, Lifetime Section, Editorial Subcommittee

W. E. Phillips, Chairman, Lifetime Section; Secretary, Subcommittee 4, Semiconductor Crystals; Crystal Perfection, Mechanical Properties of Semiconductor Surfaces, Compound Semiconductors; Impurities in Semiconductors, and Germanium Sections

A. H. Sher, Germanium Section

W. R. Thurber, Mobility, Germanium, Compound Semiconductors, and Impurities in Semiconductors Sections

ASTM Committee E-10 on Radioisotopes and Radiation Effects

W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials

J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

J. M. Kenney, Microwave Diode Measurements, Committee JC-21 on UHF and Microwave Diodes

F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11 on Mechanical Standardization; Technical Advisor, Thermal Resistance Measurements, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal and Regulator Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits

S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices

D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors

H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications, Committee JC-25 on Power Transistors

IEEE Electron Devices Group:

J. C. French, Standards Committee

J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)

H. A. Schafft, Chairman, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

IEEE Parts, Hybrids, and Packaging Group

W. M. Bullis, New Technology Subcommittee, Technical Committee on Hybrid Microelectronics

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits:

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetoresistive Devices

APPENDIX C

SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter are listed below and indicate the kinds of technology available to the program.

1. Thin Metal Films (J. Krawczyk)

Thin gold films were evaporated onto quartz plates to be subsequently etched for use as instrument scales by the NBS Microwave and Mechanical Instrumentation Section.

2. Ultrasonic Machining (J. Krawczyk)

Tapered holes were ultrasonically machined through thermocouple heads for the NBS Instrumentation Application Section.

3. Channel Electron Multipliers and Silicon Nuclear Radiation Detectors (Y. M. Liu)*

Evaluation of channel electron multipliers for the NASA Goddard Space Flight Center continued. Characterization of nine units in flight modules for the Atmospheric Explorer-C was completed.

Two commercial silicon surface-barrier detectors with keyhole-shaped electrodes and one double-grooved lithium-drifted detector were scanned with a finely-collimated beam of 1.5 MeV protons to determine edge effects in the keyhole device and cross talk between the areas delineated by the grooves on the lithium-drifted detector. These detectors are part of a series being characterized for the Mariner-Jupiter Flyby and Pioneer space packages.

4. Ribbon Wire Technology (H. K. Kessler)†

To assist the Naval Electronics Laboratory Center, San Diego, in the implementation of NBS-developed ribbon wire bonding technology, the following parts and services have been provided: technical information of and drawings for modifications to ribbon wire bonding machines, wire clamps, and tools; two mechanically modified wire clamp assemblies; a force gage assembly and a mounting assembly for magnetic pickups for use in adjusting and calibrating bonding machines; and an evaluation of several ribbon wire bonding tools.

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*NBS Cost Center 4254429

†NBS Cost Center 4254448

APPENDIX D
JOINT PROGRAM PUBLICATIONS

Prior Reports

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activity, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period since July 1, 1968, have been issued under the title Methods of Measurement for Semiconductor Materials, Process Control, and Devices. These reports may be obtained from the Superintendent of Documents (Catalog Number C.13.46:XXX) where XXX is the appropriate technical note number. Microfiche copies are available from the National Technical Information Service (NTIS), Springfield, Virginia 22151.

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December, 1968	AD 681330
December 31, 1968	475	February, 1969	AD 683808
March 31, 1969	488	July, 1969	AD 692232
June 30, 1969	495	September, 1969	AD 695820
September 30, 1969	520	March, 1970	AD 702833
December 31, 1969	527	May, 1970	AD 710906
March 31, 1970	555	September, 1970	AD 718534
June 30, 1970	560	November, 1970	AD 719976
September 30, 1970	571	April, 1971	AD 723671
December 31, 1970	592	August, 1971	AD 728611
March 31, 1971	598	October, 1971	AD 732553
June 30, 1971	702	November, 1971	AD 734427
September 30, 1971	717	April, 1972	AD 740674
December 31, 1971	727	June, 1972	AD 744946
March 31, 1972	733	September, 1972	AD 748640
June 30, 1972	743	December, 1972	AD 753642
September 30, 1972	754	February, 1973	

Current Publications:

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Copies of most of such publications are available and can be obtained on request to the editor or the author.

Phillips, W. E., Interpretation of Steady-State Surface Photovoltage Measurements in Epitaxial Semiconductor Layers, *Solid-State Electronics* 15, 1097-1102 (October, 1972).

Blackburn, D. L., Schafft, H. A., and Swartzendruber, L. J., Nondestructive Photovoltaic Technique for the Measurement of Resistivity Gradients in Circular Semiconductor Wafers, *J. Electrochem. Soc.* 119, 1773-1778 (December, 1972).

Sawyer, D. E., Prevalent Error Sources in Transistor Delay-Time Measurements, *IEEE Trans. Nucl. Sci.* NS-19, No. 6, 121-124 (December, 1972).

Thurber, W. R., Lewis, D. C., and Bullis, W. M., Resistivity and Carrier Lifetime in Gold-Doped Silicon, AFCRL Report AFCRL-TR-73-0107, January 31, 1973.

Kessler, H. K., and Sher, A. H., Microelectronics Interconnection Bonding with Ribbon Wire, NBS Tech. Note 767, April, 1973.

Sawyer, D. E., Rogers, G. J., Brewer, F. H., Leedy, T. F., Leedy, K. O., Sandow, P. M., and Huntley, L. E., Measurement of Transit Time and Related Transistor Characteristics, AFWL Report AFWL TR-73-54 (9 March 1973).

Schafft, H. A., Failure Analysis of Wire Bonds, presented as part of a Workshop on Failure Analysis of Semiconductor Devices and Packages, 1973 Reliability Physics Symposium, Las Vegas, Nevada, April 4, 1973.

Buehler, M. G., Thermally Stimulated Measurements: The Characterization of Defects in Silicon *p-n* Junctions, to be published in *Semiconductor Silicon/1973,* H. R. Huff and R. R. Burgess, eds. (Electrochemical Society, Princeton, New Jersey, 1973).

APPENDIX E

EFFECTS OF CURRENT, PROBE FORCE, AND WAFER SURFACE CONDITION ON MEASUREMENT OF RESISTIVITY OF BULK SILICON WAFERS BY THE FOUR-PROBE METHOD

Introduction — The standard set of conditions for measuring the resistivity of silicon bulk wafers with a collinear four-probe array is specified in the ASTM standard method [1]. Because variations from the standard method are common in the measurement of silicon bulk wafers in the semiconductor industry, and because of the general use of the four-probe technique for measuring the resistivity of epitaxial and diffused layers for which some of the standard conditions are inappropriate, it is useful to understand the sensitivity of the measured resistivity to variations in the measurement conditions. As a first step in developing this understanding a series of multivariable experiments on bulk silicon wafers was initiated some years ago. During the course of this work various refinements in data taking procedures were made to reduce the effect of uncontrolled variables to the greatest extent possible. Except where noted, the results reported below were taken within the past 2 years using the final set of procedures.

Experimental Procedure — Six *p*-type silicon wafers with resistivity in the range 0.001 to 100 Ω·cm, spaced at approximately decade intervals, and one *n*-type silicon with resistivity of about 100 Ω·cm were measured. Five of these wafers had been measured previously as part of an interlaboratory test [2] to validate the conditions and precision specified in the ASTM method [1]. In the present case measurements were made on each of the seven test wafers at all combinations of surface condition, probe force, and current level in a specified sequence of values for each variable. Three surface conditions (mechanically polished with 0.3-μm alumina, chem-mechanically polished [3], and lapped with 5-μm alumina), four probe forces (25, 40, 100, and 150 grams force per pin*), and five current levels (0.1, 0.22, 1.0, 2.2, and 10† times the specified current, I_0, for each wafer (NBS Tech. Note 555, p. 6, [1])) were used in the measurements. Measurements were first made on mechanically polished surfaces in the following sequence. Starting with a probe force of 25 gf and a current of 0.1 I_0, the room temperature resistivity was measured at the center of each wafer at 12 approximately equiangular (∿30 deg) intervals, and the average and sample standard deviation computed. The set of 12 measurements was repeated, at the same value of probe force, for the currents I_0, 10 I_0, 2.2 I_0, and 0.22 I_0. The staggered ordering of the current was chosen to separate temporal effects from

*0.24, 0.39, 0.98, and 1.47 newton per pin, respectively.

†No measurements at 10 I_0 were made on the 0.001- and 0.01-Ω·cm wafers because of heating effects at the probe tips (NBS Tech. Note 555, p. 7).

current level effects. After the five sets were completed for the lowest value of probe force, the sequence was repeated for each of the next higher values of probe force. All wafer surfaces were then chem-mechanically polished and the entire sequence was repeated. Lastly, the wafer surfaces were lapped, and the entire sequence was repeated again.

Every effort was made to ensure that the equipment used in this experiment met all the electrical and mechanical requirements of the ASTM standard [1]. Considerable time was spent to assure the quality of the probe tips and of the electronics. Temperature in the test room was maintained between 22 and 24°C so that the standard correction for temperature [1] could be applied. Otherwise, it is believed that the measurement conditions included in the study covered as great a range of operating conditions as would be experienced in industrial application of the four-probe method. Difficulties were encountered in assuring the cleanness of wafer surfaces measured several days after preparation of the surface condition and in identifying and correcting for hidden variables. The second difficulty confused the meaning of much of the data taken early in the study and led eventually to the measurement sequence described earlier.

Results — It was intended at the outset to examine the data for two results:

1. conditions for which the average resistivity obtained differed by 1 percent or more from the value obtained under standard conditions [1], and
2. conditions for which the relative sample standard deviation for a set of 12 measurements was significantly greater than the 0.25 percent which could be obtained for most wafers under standard conditions.

The second result is significant with respect to typical single-measurement, accept/reject tests made in the industry; increased variability would reduce the confidence which could be placed on pass/fail tests based on one datum.

The overall quality of the data obtained can be most succinctly described if the less stable data, taken with probe force of 25 gf or current level of 0.1 I_0, are excluded. Then, for each wafer except the 1-Ω·cm wafer, all average resistivity values as measured above fell within ±1 percent of the grand average, although this average was different from that measured under standard conditions [1]; for the 1-Ω·cm wafer, the range was ±1.2 percent. For no set of 12 measurements did the relative sample standard deviation exceed 0.4 percent within the restrictions just stated.

A more formal analysis of the data is difficult because none of the observed effects from any of the variables was very large. Those that were distinguishable were generally modified by interactions with one of the other variables or were observed only on a single wafer rather than displaying a functional dependence on

Table 5 — Qualitative Summary of Effects of Surface Condition, Current, and Probe Force on Four-Probe Resistivity Measurements

Effect of	On[a]	Specimen 612522 (∿0.001 Ω·cm)	600200 (∿0.01 Ω·cm)	607075 (∿0.1 Ω·cm)	325 (∿1 Ω·cm)	49445 (∿10 Ω·cm)	66966 (∿100 Ω·cm)	71983[b] (∿100 Ω·cm)
Surface Condition	$\bar{\rho}$[c]	M>L>C	M>L>C	M>L=C	M>C>L	M>C>L	M>L>C	M>L>C
	s	——	——	——	——	——	increased scatter on polished surfaces at low current, probe force	increased scatter on polished surfaces at low current, probe force
Current	$\bar{\rho}$	reduced number of significant figures at 0.1 I_0	——	slight decrease with increasing current	——	sudden increase at 10 I_0	——	slight increase with increasing current
	s	increased scatter at 0.1 I_0	——	——	——	——	increased scatter at 0.1 I_0	increased scatter at 0.1 I_0
Probe Force	$\bar{\rho}$	——	——	current effects reduced at higher probe force	——	current effects reduced at higher probe force	——	——
	s	——	——	——	——	——	increased scatter at 25 gf	increased scatter at 25 gf

a $\bar{\rho}$ = average resistivity, s = sample standard deviation of sets of 12 measurements

b specimen is *n*-type; all others, *p*-type

c M = mechanically polished, L = lapped, C = chem-mechanically polished

resistivity. Although no generalized quantitative statement of effects can be extracted from the analysis, several qualitative observations can be made. These are discussed below and summarized in table 5.

Current level had no effect on the variance of a set of 12 measurements except that for the lowest and highest resistivity levels measurements made with a current of 0.1 I_0 had considerably greater scatter than usual. Only two wafers showed an effect of current level on the average value: The average resistivity of the 0.1-Ω·cm wafer decreased slightly with increasing current; this was complicated by a hysteresis in the current dependence which diminished as the probe force increased. The resistivity of the 10-Ω·cm wafer was essentially constant at the four lowest current levels but increased as much as 1.5 percent at a current of 10 I_0 and probe force of

25 gf; this increase was smaller at larger values of probe force and varied somewhat with surface condition.

Probe force had no effect on the average value of the resistivity of any of the wafers except through the moderation of the current dependence of the resistivity of two wafers as discussed above. Effects of probe force on the variance were in evidence only for the two 100-Ω·cm wafers where extensive scatter was encountered frequently at a probe force of 25 gf and occasionally at 40 gf. For one set of 12 measurements at a current of 0.1 I_0 and a probe force of 25 gf on the 100-Ω·cm, *p*-type wafer, the relative sample standard deviation was 11 percent.

Surface condition had little effect on variance of data sets except that the two 100-Ω·cm wafers showed a rather strong tendency toward erratic readings for both mechanically and chem-mechanically polished surfaces. On the other hand, of all the variables, surface condition appeared to be the one having the greatest effect on average resistivity level; differences of a few tenths percent or more were observed between measurements made with various surface conditions on all wafers. However, an ongoing study of the resistivity stability of two other wafers which have been measured every two weeks for about a year using only a single set of measurement conditions shows a range of values about ±0.5 percent about the mean of each. Since this range is comparable to that observed for the three surface preparations for which data were taken over a period of nearly a year, changes in measured resistivity with changing surface condition cannot be unambiguously attributed to the change in surface condition. This difficulty of comparing average values for the various surface conditions was further confirmed by remeasurements made under selected combinations of conditions. The results of these measurements showed the same short-term current and probe force behavior as the original set taken under the same conditions, but the values for the mean resistivity generally differed from the original. These results are more suggestive of long-term variability in the measurement process rather than of a unique correspondence between surface condition and average resistivity.

Attempts at formal analysis of variance to obtain the dependence on measurement variables were largely inconclusive. The few tests which yielded results which appeared to be statistically significant were generally discarded because the dependences observed were generally not monotonic functions of the variable concerned and appeared to be due to the formatted procedure for taking the data. Nonparametric tests of concordance yielded results similar to the analysis of variance.

Values of average resistivity, sample standard deviation, and relative sample standard deviation for selected groupings of data are listed in table 6. Each of the first three groups includes data taken for one surface condition in the sequence described above. Within each group, measurements made at all values of current and

APPENDIX E

Table 6 — Pooled Results for Selected Combinations of Data

Group	Quantity	Specimen						
		612522	600200	607075	325	49445	66969	71983[a]
1	ρ, Ω·cm	0.0009807	0.007781	0.10922	1.0972	11.885	112.16	100.85
	s, Ω·cm	0.0000087	0.000056	0.00068	0.0090	0.062	1.06	0.92
	s, %	0.89	0.72	0.62	0.82	0.52	0.95	0.91
2	ρ, Ω·cm	0.0009761	0.007758	0.10856	1.0969	11.826	112.47	100.40
	s, Ω·cm	0.0000030	0.000011	0.00034	0.0017	0.052	0.55	0.65
	s, %	0.31	0.14	0.31	0.15	0.44	0.49	0.65
3	ρ, Ω·cm	0.0009857	0.007775	0.10873	1.0843	11.794	112.50	100.36
	s, Ω·cm	0.0000071	0.000018	0.00052	0.0031	0.043	0.41	0.10
	s, %	0.72	0.23	0.48	0.29	0.36	0.36	0.10
4	ρ, Ω·cm	0.0009799	0.007772	0.10884	1.0931	11.838	112.40	100.55
	s, Ω·cm	0.0000076	0.000038	0.00060	0.0083	0.066	0.68	0.68
	s, %	0.78	0.49	0.55	0.76	0.56	0.60	0.68
	Number[b]	87	65	156	80	80	122	85
5	ρ, Ω·cm	0.0009803	0.007748	0.10801	1.0911	11.829	112.21	101.05
	s, Ω·cm	0.0000089	0.000073	0.00290	0.0083	0.069	0.94	2.85
	s, %	0.91	0.94	2.68	0.76	0.58	0.84	2.82
	Number[b]	135	127	223	110	140	185	153
6	ρ, Ω·cm	0.000981	0.007785	0.10905	1.0854	11.783	112.72	100.33
	s, Ω·cm	0.0000012	0.000019	0.00017	0.0020	0.030	0.10	0.14
	s, %	0.12	0.24	0.16	0.18	0.25	0.09	0.14
7	ρ, Ω·cm		0.007763	0.10909		11.869	113.06	101.08
	s, Ω·cm		0.000032	0.00037		0.075	1.03	0.64
	s, %		0.41	0.34		0.63	0.91	0.63
8	ρ, Ω·cm		0.007743	0.10881		11.877	112.59	100.6
	s, Ω·cm		0.000017	0.00017		0.023	0.28	0.38
	s, %		0.22	0.16		0.19	0.25	0.38

[a] specimen is *n*-type; all others, *p*-type

[b] number of measurement sets

probe force are pooled; replicate measurements, which were made for some conditions, are also included. The fourth group is a consolidation of the first three. The fifth group includes all the data of the fourth group plus a large amount of data previously acquired on lapped surfaces with a more loosely arranged format. The sixth group is a single set of 12 measurements made on each wafer under standard conditions [1] (lapped surface, current of I_0, and probe force of 150 gf). The seventh and eighth groups are, respectively, the multilaboratory and NBS values obtained in the previous interlaboratory test [2].

Since the longer term temporal effects have been seen to be of the same order as the largest of the effects directly studied in this experiment and since a large number of repetitive measurements were not made to distinguish between time and surface dependent effects, it is not valid to infer statistical tolerance limits on the range which might be expected for data taken under a given set of conditions solely from the data acquired in this experiment. However, several definite conclusions may be drawn from this experiment. The sample standard deviations tabulated in the fourth group of table 6 (consolidated results for three surface conditions) are generally comparable to those obtained in the interlaboratory test made under rigidly fixed conditions. Taking the former as representative of the variation of measurement averages to be encountered over a wide range of measurement conditions, it appears that the four-probe method is very robust against variation of the mean with changing measurement conditions. Further, as has been noted, except for a few measurement conditions, relative sample standard deviation on any set of measurements never exceeded 0.4 percent. This value is judged to be a realistic measure of the short term precision attainable for four-probe resistivity measurements using equipment which meets the requirements of the standard method [1]. The implication of this precision value is that one may state with 90 percent confidence that 90 percent of all single measurement pass/fail data taken will fall within a range no greater than ±1 percent of the value obtained by averaging 12 readings under the same conditions of measurement. The only measurement conditions which were excepted from the above and which should be used with caution, if at all, were the low current level (0.1 I_0) and low probe force (25 gf) conditions. Particularly at very high and very low specimen resistivities, use of low current resulted in situations of low signal or low signal-to-noise ratio and use of low contact force resulted in greater susceptibility to vibration and increased contact impedance. Finally, although for 10-Ω·cm and lower resistivity material both types of polished surfaces yielded values for relative standard deviation fully as low as those from lapped surfaces, lapped surfaces proved to be considerably more stable for 100-Ω·cm material of either conductivity type.

(J. R. Ehrstein, F. H. Brewer, D. R. Ricks, and W. M. Bullis)

REFERENCES

1. Standard Method for Measuring Resistivity of Silicon Slices with a Collinear Four-Probe Array, ASTM Designation F84-72, *Annual Book of ASTM Standards*, Part 8. Available as a separate reprint from American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pa. 19103.

2. Bullis, W. M., Standard Measurements of the Resistivity of Silicon by the Four-Probe Method, NASA-CR-86032, 29 December 1967. Available from National

Technical Information Service, Springfield, Virginia 22151, Accession Number N68-18067.

3. La Chapelle, R., Composition for Polishing Crystalline Silicon and Germanium and Process, U.S. Patent 3,429,080, February 25, 1969.

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16. ABSTRACT (A 200-word or less factual summary of most significant information. If document includes a significant bibliography or literature survey, mention it here.) This quarterly progress report, eighteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include (1) completion of the investigation of the effects of current, probe force, and surface condition on the measurement of resistivity of bulk silicon wafers by the four-probe method, (2) establishment of operating conditions appropriate for determining the sensitivity of transient thermal response measurements to voids in transistor die attachment, and (3) initiation of an interlaboratory comparison of transistor scattering parameter measurements. Because of the general applicability of the first of these, details are presented in a separate appendix. Work is continuing on measurement of resistivity of semiconductor crystals; characterization of generation-recombination-trapping centers in silicon; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; measurement of thermal properties of semiconductor devices; determination of S-parameters, delay time, and related carrier transport properties in junction devices; development of a-c probing techniques; and characterization of noise and conversion loss of microwave detector diodes. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendices.

17. KEY WORDS (Alphabetical order, separated by semicolons) Base transit time; carrier lifetime; delay time; die attachment; electrical properties; electronics; epitaxial silicon; four-probe method; generation centers; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; probing techniques (a-c); pull test; recombination centers; resistivity; resistivity standards; semiconductor devices; semiconductor materials; semiconductor process control; silicon; S-parameters; switching transients; thermal resistance; thermally stimulated measurements; trapping centers; wire bonds.

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